AlGaN/GaN High Electron Mobility Transistors Grown by MOVPE on 3C-SiC/Si(111) for RF Applications

Marie Lesecq, Eric Frayssinet, Marc Portail, Micka Bah, N. Defrance, Thi Huong Ngo, Mahmoud Abou Daher, Marcin Zielinski, Daniel Alquier, Jean-Claude de Jaeger, et al.

Materials Science Forum
ISSN: 1662-9752, Vol. 1062, pp 482-486
doi:10.4028/p-2wi7o8

Submitted: 2021-10-11
Revised: 2022-02-14
Accepted: 2022-03-17
Online: 2022-05-31

AlGaN/GaN High Electron Mobility Transistors Grown by MOVPE on 3C-SiC/Si(111) for RF Applications

Marie Lesecq[1,a], Eric Frayssinet[2,b], Marc Portail[2,c], Micka Bah[3,d], Nicolas Defrance[1,e], Thi Huong Ngo[2,f], Mahmoud Abou Daher[1,g], Marcin Zielinski[4,h], Daniel Alquier[3,i], Jean-Claude De Jaeger[1,j] and Yvon Cordier[2,k*]

[1]Univ. Lille, CNRS, Centrale Lille, Univ. Polytechnique Hauts-de-France, UMR 8520 – IEMN-Institut d'Electronique de Microélectronique et de Nanotechnologie, F-59000, Lille, France

[2]Université Côte d'Azur, CNRS, CRHEA, rue B.Grégory, 06560 Valbonne, France

[3]GREMAN, Université de Tours, INSA Centre Val de Loire, 37071 Tours, France

[4]NOVASiC, Savoie Technolac, 73370 Le Bourget-du-Lac, France

[a]marie.lesecq@univ-lille.fr, [b]ef@crhea.cnrs.fr, [c]mpo@crhea.cnrs.fr, [d]micka.bah@univ-tours.fr, [e]nicolas.defrance@univ-lille.fr, [f]thn@crhea.cnrs.fr, [g]mahmoud.abou-daher@univ-lille.fr, [h]mzielinski2012@gmail.com, [i]daniel.alquier@univ-tours.fr, [j]jean-claude.de-jaeger@univ-lille.fr

[*]corresponding author: [k]yvon.cordier@crhea.cnrs.fr

Keywords: Epitaxy, GaN HEMT, high frequency.

Abstract. In this work, an AlGaN/GaN HEMT structure is grown on a 0.8 µm thick 3C-SiC layer on high resistivity Silicon substrate. The RF propagation losses are investigated and compared with the ones of epi-layers grown directly on Silicon and on 6H-SiC substrates. Short gate length transistors are fabricated using e-beam lithography. In spite of ohmic contact resistance of 0.6 Ω.mm, a saturated current density of 0.7 A/mm at a gate bias of +1V and a transconductance peak higher to 250 mS/mm for 75 nm T-shaped gate transistors are reached on structure with thick 3C-SiC template. Moreover, for the first time, transition frequencies f_T/f_{max} of 60/98 GHz are reported on such 3C-SiC template.

Introduction

Gallium nitride based devices show clearly their outstanding performances for microwave power applications. These performances are strongly linked with the properties of the substrate used for the epimaterial growth. Best performances are obtained on GaN-on-SiC (Silicon Carbide) devices [1] but SiC substrates suffer from lower availability compared to Silicon ones permitting also to get GaN devices with interesting high frequency performances [2]. However, these last devices still suffer from the difficulty to grow high crystal quality crack-free RF compatible GaN based epilayers. Typically, AlGaN/GaN epilayer High Electron Mobility Transistor (HEMT) structure starts with the growth of an AlN nucleation layer. The growth parameters of this layer strongly influence the propagation losses due to the risk of diffusion of Al and/or Ga into the Si substrate [3-4]. It has been reported that the use of cubic (3C-SiC) intermediate layer as a template for the growth of AlGaN/GaN HEMT heterostructures on Si substrate limits the risks of cracks generation, enhances the crystal quality of the GaN film [5-6] and limits the degradation of Silicon substrate resistivity permitting to preserve low RF propagation losses [7]. RF performances were reported on AlGaN/GaN HEMTs on 3C-SiC/Si substrates using an ultrathin 3C-SiC intermediate layer deposited by CVD (Chemical Vapor Deposition) followed by AlGaN/GaN growth by MOCVD (Metal Organic Chemical Vapor Deposition). A current gain cut off frequency (f_T) of 176 GHz and a maximum oscillation frequency (f_{max}) of 70 GHz were obtained on an 80 nm-rectangular gate length device [8]. Furthermore, f_t and

f_{max} of 110 GHz were obtained on 100 nm tri-gate devices associated with an I_{ON}/I_{OFF} ratio of 10^8 [9]. Beyond these achievements, the thickening of the 3C-SiC intermediate layer seems to be promising to improve the thermal dissipation, to reduce the propagation losses and to increase the RF performance. Relatively low losses can be obtained on HEMT buffer layers grown on Si with a thick 3C-SiC intermediate layer despite the limited initial resistivity of the substrate [7,10] but the demonstration of high frequency performance transistors fabricated on such thick template is still lacking.

Material Growth and Device Technology.

Intrinsic Silicon substrate with an initial resistivity higher than 5 kOhm.cm is used as a starting substrate. Then, a 0.8 µm thick 3C-SiC transition layer is grown at around 1300°C by CVD on this substrate. After a chemical mechanical polishing of the 3C-SiC template, the AlGaN/GaN HEMT structure is grown by MOCVD using conditions previously described in [7]. The epitaxial structure consists of a 1µm-thick GaN buffer layer on a 1.2 µm thick AlGaN/AlN stress accommodation sequence (Fig.1) and followed by an $Al_{0.26}Ga_{0.74}N$ barrier capped with 3 nm-thick SiN layer. A 1nm-thick AlN exclusion layer is used to reduce alloy scattering and improve carrier confinement within the two-dimensional electron gas (2DEG). For comparison purposes, a similar AlGaN/GaN heterostructure is grown on a high-resistivity bulk 6H-SiC substrate.

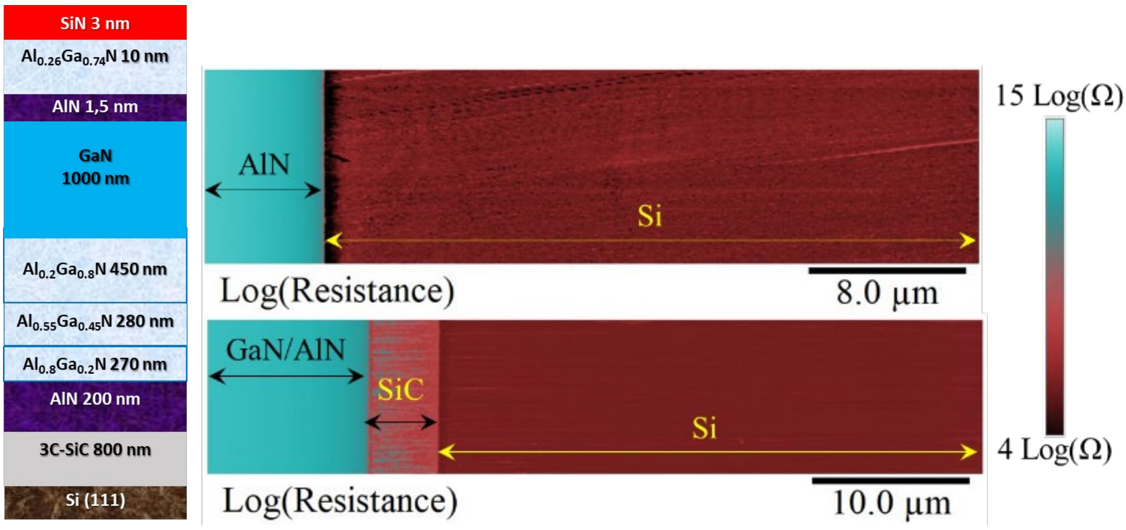

Figure 1. (left) Cross section picture of the HEMT structure grown on 3C-SiC/Si; (right) Top: scanning spreading resistance microscopy (SSRM) showing the resistivity drop at AlN/Si interface. Bottom: absence of resistivity drop at AlN/3C-SiC and 3C-SiC/Si interfaces

Before the device process, the electrical properties of epilayers are first evaluated with contactless sheet resistance measurements using an Eddy current setup and with mercury-probe Capacitance-Voltage (Hg-CV). The electrical behaviour of the AlN and 3C-SiC epi-layers is studied via scanning spreading resistance microscopy (SSRM) on a bevelled sample as described in [4]. Propagation losses are measured in the 0.25-67 GHz frequency range on coplanar waveguides fabricated on the epilayer after N+ ion implantation for isolation. E-beam based technological process is performed to fabricate short gate length devices. A Ti/Al/Ni/Au metal stack annealed at 850°C for 30 s is used to form the source and drain ohmic contacts. Ni/Au T-shaped Schottky gates are then defined. A 100nm Si_3N_4 layer is deposited by PECVD as final passivation. To assess the 2DEG low field transport properties, Hall effect measurements are performed on-wafer on Van der Pauw patterns defined nearby transistors.

Results and Discussion.

Table 1 compares the RF propagation losses measured at 40 GHz in the present HEMT with ones of structures grown with a single stress mitigating layer (350 nm thick $Al_{0.26}Ga_{0.74}N$) on 3C-SiC/Si(111) or directly on Si(111). Losses are also reported for a HEMT structure grown with a 2.5 µm thick GaN buffer layer on 6H-SiC. In the present cases, propagation losses are mainly due to parasitic conduction in the epilayers and/or in the substrate. Our previous study of layers grown directly on Silicon has shown that Gallium was mainly responsible for the detrimental reduction of electrical resistivity at the AlN/Si interface [4]. As shown in table 1, losses obtained on 3C-SiC are noticeably lower than those on the structure grown directly on Silicon. It can be also noted that, the insertion of a thicker stack with three AlGaN steps in the present HEMT buffer layer did not change the losses which are around 0.4 dB/mm at 40 GHz. Furthermore, the 0.25 dB/mm losses obtained on the structure on semi-insulating 6H-SiC clearly illustrate the better stability of such substrate against parasitic doping with III-metal elements during the nucleation and growth of the III-Nitride epilayers.

Table 1. Propagation losses at 40 GHz in the epi-layers grown on Si(111), 3C-SiC/Si templates and 6H-SiC substrate.

Grown structure	Substrate resistivity [ohm.cm]	Losses at 40 GHz [dB/mm]
GaN on Si(111)	> 5000	1.2
GaN on 3C-SiC/Si(111)	> 5000	0.38
HEMT on 3C-SiC/Si(111)	> 5000	0.41
HEMT on 6H-SiC	semi-insulating	0.25

The SSRM analysis of the lower parts of structures grown on Silicon and on 3C-SiC/Si are compared in Fig.1. Contrary to the layers grown directly on Silicon, no drop of electrical resistivity is noticed at the AlN/3C-SiC interface, nor at the interface between 3C-SiC and Silicon. This analysis confirms the macroscopic resistivity measurements revealing sheet resistances below 4 kΩ/sq typically for direct growth on Silicon while they overpass 10 kΩ/sq on the present 3C-SiC/Si templates. Hg-CV performed on the present HEMT grown on 3C-SiC indicates a 2DEG charge density close to $7.8x10^{12}$ cm^{-2} confirmed by Hall effect measurements revealing a high electron mobility near 2000 cm^2/V.s and a sheet resistance of 392 Ω/sq. The HEMT heterostructure grown on 6H-SiC exhibits a 2DEG density of $8.2x10^{12}$ cm^{-2} and a sheet resistance around 345Ω/sq.

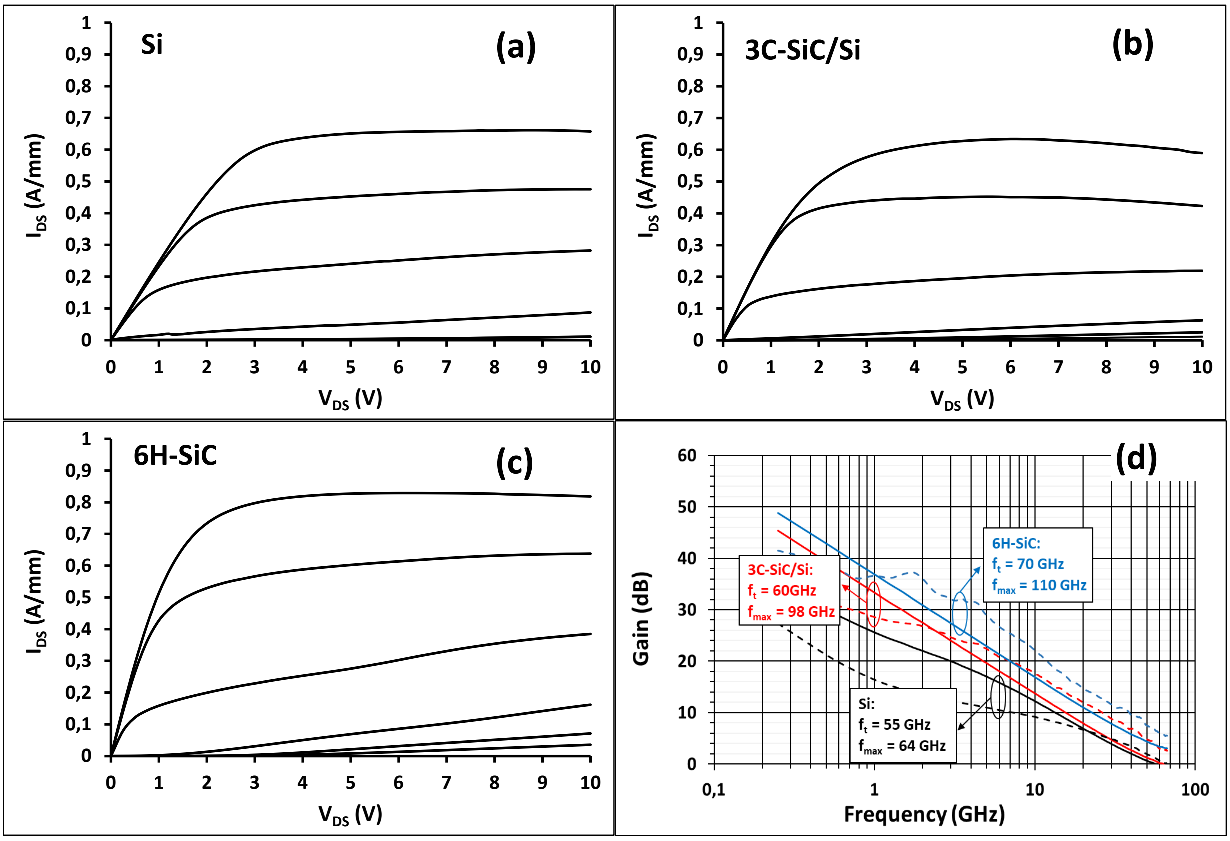

Figure 2. DC output characteristics of a 2 x 50 µm x 0,075 µm gate transistor fabricated on the AlGaN/GaN HEMT heterostructure grown on (a) Si(111), (b) 3C-SiC/Si(111) and (c) 6H-SiC (V_{gs}=0V to -5V, V_{gs} steps = -1V). (d) comparison of gains measured on the transistors.

Devices under test (DUT) in this work feature a two-finger configuration with a gate width (W) of 50µm, a gate length (L_G) of 75 nm and a source-to-drain spacing (L_{SD}) of 1.5 µm. Fig.2. shows the DC output characteristics $I_{DS}(V_{DS})$ of the devices. On 3C-SiC/Si, a knee voltage under 3 V and a clear saturation of the drain current are obtained. A saturated current density of 0.65 A/mm is reached at a gate bias V_{GS}=0V. The peak transconductance g_m is 260 mS/mm at V_{DS}=4V and V_{GS}=-1.7V. A threshold voltage V_{th} of -3.2 V is deduced from the transfer characteristic (not shown). The gate leakage current is as low as 10^{-8} A/mm. On 6H-SiC, a saturated current density of 0.8 A/mm is obtained at V_{GS}=0V. The peak transconductance g_m is 330 mS/mm at V_{DS}=4V and V_{GS}=-1.7V. The ohmic contact resistance around 0.6 Ω.mm is the same on both HEMT structures. The current gain transition frequency (f_T) and the maximum oscillation frequency (f_{max}) are directly extracted from the first order frequency extrapolation (−20 dB/decade) of current gain modulus ($|H_{21}|$) and Mason's unilateral gain (U) respectively for a bias point corresponding to the maximum of transconductance. On 3C-SiC/Si, at V_{DS}=4V and V_{GS}=-1.7V, extrinsic current gain cutoff frequency f_t = 60 GHz and maximum power gain cutoff frequency f_{max}= 98 GHz are obtained. On 6H-SiC, slightly higher transition frequencies f_t=70 GHz and f_{max}=110 GHz are obtained at V_{DS}=4 V and V_{GS}=-1.7V. These performances are limited by the ohmic contact resistance and the sheet carrier density correlated with the low (26%) Al content regarding the thickness of the AlGaN barrier (10 nm) as well as by some trapping effects. On Si, f_t = 55 GHz and f_{max}= 64 GHz. The increase of the Al content up to 29% [11] combined with a well-suited passivation step may result in improved microwave performance.

Conclusion.

In this work, AlGaN/GaN HEMT structures are grown by MOCVD on different substrates. Compared with direct growth on Silicon substrate, a clear benefit appears in terms of electrical resistivity for buffer layers grown on thick 3C-SiC/Si templates resulting in reduced RF propagation losses.

Transistors fabricated on such template show performances close to those obtained on semi-insulating bulk SiC substrates, with in particular a maximum oscillation frequency of 100 GHz confirming the interest of these devices for high-frequency applications at reduced cost.

Acknowledgments.

This work was supported by the technology facility network RENATECH and the French National Research Agency (ANR) through the projects ASTRID GoSiMP (ANR-16-ASTR-0006) and the "Investissement d'Avenir" program GaNeX (ANR-11-LABX-0014). This research work has been partially undertaken with the support of IEMN fabrication (CMNF) and characterization (PCMP).

References

[1] K. Harrouche et al, Journal of the Electron Devices Society 7 (2019) 1145.

[2] P. Cui et al, Applied Physics Express 12 (2019) 104001.

[3] S. Chang et al, Semiconductor Science and Technology 35 (2020) 035029.

[4] M. Bah et al, Scientific Reports 10 (2020) 14166.

[5] Y. Cordier et al, Journal of Crystal Growth 310 (2008) 4417.

[6] S. Leone et al, Journal of Applied Physics 125 (2019) 235701.

[7] E. Frayssinet et al, Phys. Status Solidi A 217 (2020) 190060.

[8] W. Jatal et al, IEEE Electron Device Letters 36 (2015) 123.

[9] W. Jatal, et al, Phys. Status Solidi A 214 (2017) 415.

[10] A. Bose et al, IEEE Electron Device Letters, 41 (2020) 301948.

[11] E. Frayssinet et al, Phys. Status Solidi A 214 (2017) 1600419.