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# Ageing of glass passivated TRIAC devices under thermal and electrical stress

Y. Buvat, E. Bouyssou, B. Morillon, G. Gautier

*Abstract – A new silicate glass passivation was studied on Metal-Dielectrics-Semiconductor structures to characterize the reliability performances of TRIAC devices. The presence of mobile ions was identified in the glass affecting the reliability performances. The addition of a semi-insulating passivation layer turns out to drastically improve the reliability performances of TRIAC devices.*

## 1. Introduction

Several type of power electronic switches, such as diodes, transistors, thyristors or TRIAC devices (Triode for Alternating Current), exist on the market with their benefits and withdraws. Thyristors and TRIAC devices are bidirectional semiconductor switches and are considered as power devices. They can be found in a variety of applications such as household electrical appliances (e.g. washing machines, cookers, coffee machines...), AC loads drive and more recently in industrial sector [1] as well as automotive market [2] with the electrification of vehicles.

TRIAC devices must withstand high voltage with low leakage current during the OFF state and conduct enough current with minimum loss during the ON state. The die edge termination, also called “periphery” is the device part dedicated to the OFF state. So, its properties are strongly correlated with the blocking performances of the device. TRIAC devices are manufactured through three main technologies which are closely based on the edge termination as illustrated in Figure 1: “planar,” “top glass,” and “double mesa” [3]. These technologies are a result of various trade-offs between cost and device performances. The “planar” technology enables to reach good electrical performances, but it remains relatively expensive, due to its large periphery area. However, “top glass” technology and even more “double mesa” technologies are cost effective and have been demonstrated to yield high blocking voltage with a limited periphery area.

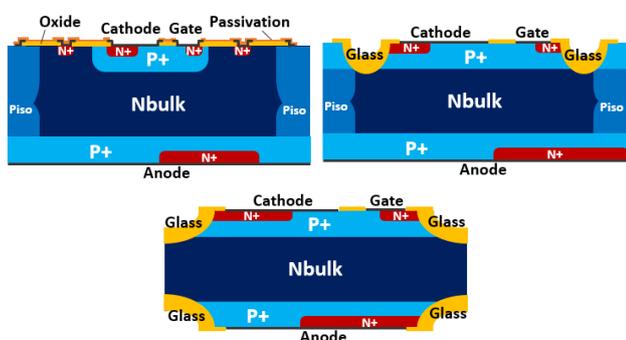


Fig. 1. Simplified diagrams of planar technology (left), top glass technology (right) and double mesa technology (center)

TRIAC devices usually work at environment temperatures from 60°C up to 80°C but the junction temperature can reach higher levels when dealing with high power during ON state. In addition, new applications of TRIAC require to withstand higher temperature and excellent reliability performances. So, even if TRIAC devices technologies can be considered as mature, some research is still performed to improve reliability by adding a stop channel [5] or searching for new dielectric passivations [6-7]. Some work has been done also to reach a better cost-effective technology by reducing the periphery area of planar structure [4].

The die termination of mesa glass devices consists in a groove which is passivated with a specific silicate glass containing metallic oxides such as lead oxide; silicate glass is generally effective for achieving good reliability performances in high voltage silicon power devices. Charges existing in the passivation layer are known to influence the electrical and reliability behaviour when subjected to thermal and electrical stress [8]. Also, the functional reliability of the device can be altered by the presence of mobile ion in the passivation [9]. Consequently, the failure of TRIACs should be studied and monitored by the means of accelerated lifetime tests and by observing the time evolution of leakage current. Moreover, the stability of the latter is crucial in order to avoid thermal runaway during the device operation.

Finally, new environmental regulation on electronic component specifies that hazardous materials such as lead are forbidden, which implies that substitute materials must be used. Few alternatives exist to remove lead in passivation layer. The use of other silicate glasses [10-12] is considered as a best option, as it is close to the existing solution.

Considering the new TRIAC devices application requirements and the new environmental regulations, a new silicate glass was studied. Hence, the aim of this paper is to characterize the electrical charges in this new silicate glass passivation and evaluate the impact on reliability performances of TRIAC devices.

## 2. Experimental procedure

Two kinds of test vehicles were processed: Metal-Glass-Semiconductor (MGS) structures, to characterize the electrical

behaviour of glass material, and TRIAC devices in order to perform the glass reliability assessment on final products.

### 2.1. MGS structures

Metal-Glass-Semiconductor structures (fig.2) were processed on 150 mm N type silicon substrates with a resistivity of 33-39 Ohm.cm in order to characterize the glass material. Powder glass mixed with a photoresist is first deposited by spin coating technique, followed by a pyrolysis at 500°C to remove the resist. Finally, a firing step is done in order to melt glass powder and to form an amorphous glass layer. Aluminum electrodes are then evaporated directly on glass film before backside metallization. The final thickness of the glass film is 8 µm and the aluminum electrodes area is 25 mm<sup>2</sup>.

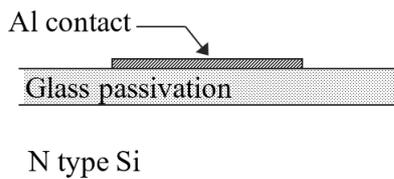


Fig. 2. Schematic cross section view of an MGS structure

### 2.2. TRIAC devices

The use of silicate glass as a passivation is known to eventually influence the level of leakage current due to additional carrier generation/recombination at the silicon-glass interface [12,13]. Consequently, two sets of TRIAC devices were manufactured: one set with the new glass material as unique passivation layer and one set with a combination of a semi-insulating layer and the new glass material. The semi-insulating layer has been deposited using chemical vapor diffusion technique with a gas combination of SiH<sub>4</sub>/N<sub>2</sub>O. The thickness of the semi resistive layer is 500 nm. Wang *et al.* [7] reported that any undesired charges disturbing the electric field distribution can be compensated by the semi-insulating layer.

The reliability test at package level is not the best solution as we want to study the behavior of the silicate glass passivation without any interaction with a packaging effect. Indeed, Lantz *et al.* [14] reported the potential impact of the encapsulation resin on the reliability performances due to the presence of mobile ions. Therefore, TRIAC dies have been especially soldered on a silicon substrate (fig.3) in order to perform electrical reliability tests using a semi-automatic probe-station.

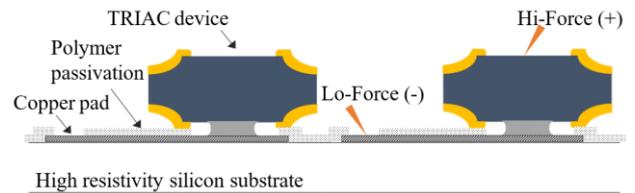


Fig. 3. Cross section view of TRIAC dies soldered on a silicon substrate

## 3. Measurement procedures

### 3.1. Capacitance-Voltage measurement

Capacitance-Voltage (CV) measurements were performed using a 4200 Semiconductor Parametric analyzer associated with an external 2657A high voltage Source Measure Unit and a high voltage bias tee. The voltage sweep was performed between -500 V to 500 V at 1 MHz.

### 3.2. Bias Temperature Stress method

Bias Temperature Stress (BTS) was performed at wafer level to identify the presence of mobile ions and evaluate their effect on the blocking performances. This test consists in stressing the Metal-Glass-Semiconductor structure by applying a DC voltage at high temperature using a semi-automatic probe station associated with a temperature regulated chuck and performing Capacitance-Voltage readout measurements at ambient temperature (fig.4). Several Bias Temperature Stress tests were appended up to 220 h in order to observe the evolution of TRIAC devices key parameter. At the end of the test, 26 Capacitance-Voltage readout measurements were performed.

The aging tests were performed from 100°C up to 150°C, for voltage stress levels ranging between 300 V and 700 V. The equivalent electrical field applied in the new glass in the Metal Glass Semiconductor is calculated between 375 kV/cm and 875 kV/cm respectively.

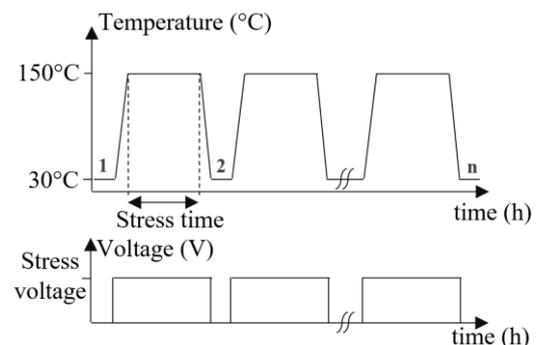


Fig. 4. Diagram of BTS and DC HTRB method. At ambient temperature either CV or IV readout measurement are performed.

### 3.3. Die reliability method

The die reliability method employed is a DC High Temperature Reverse Bias test (HTRB) and is quite similar to the Bias Temperature Stress method except that Current-Voltage (IV) characteristics are performed instead of Capacitance-Voltage measurement (fig 4). Moreover, the time evolution of the leakage current is recorded during the stress period. A custom program was made to regulate the temperature and control the test instruments and the semi-automatic probe-station.

Like other power devices, TRIAC devices are sensitive when applying DC stress at high temperature. If the leakage current is too high, the TRIAC devices are likely to switch in ON state. That is why the voltage stress applied was fixed at 100V, which correspond to an electrical field of 33 kV/cm simulated by TCAD (Technology Computer Aided Design) tool as illustrated in figure 5. Consequently, the voltage acceleration effects will not be studied on TRIAC devices. The temperature stress was fixed between 120°C and 160°C.

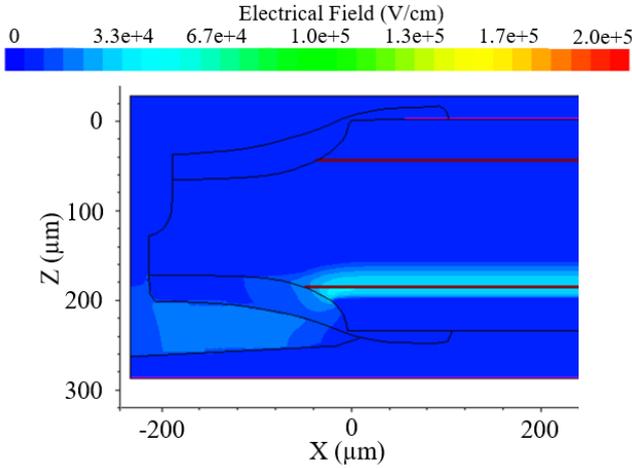


Fig. 5. TCAD simulation of generated electrical field along the glass-silicon interface when applying 100 V across a TRIAC device.

## 4. Results and discussion

In this part, the capacitance-voltage behavior will be explained. Then, the results on the voltage stress and the temperature stress effects of the Metal Glass Semiconductor structure and the TRIAC devices will be shown. At last, the addition of a semi-resistive layer between the new glass and the silicon in TRIAC devices will be explained and discussed regarding the reliability performances.

### 4.1. Capacitance-voltage

First, a Capacitance-Voltage measurement (fig.6) can give us information on the presence of charge in the glass. It is well known that the initial shift of the Capacitance-Voltage curve towards the voltage axis compared with a theoretical curve indicates a presence of charges in the dielectric.

In a MGS structure, the energy band of the semiconductor is considered flat for a specific voltage bias. This specific voltage bias is called the flat-band voltage. Charge density at the flat-band equilibrium can be extracted from CV measurements by the following formula [15]:

$$N_{FB} = \frac{C_{OX}(W_{MS} - V_{FB})}{q \times A} \quad (1)$$

where  $W_{MS}$  is the contact potential difference in MGS structure [V],  $C_{OX}$  is dielectric capacitance [F/cm<sup>2</sup>],  $V_{FB}$  is the flat-band voltage [V],  $q$  the elementary charge [C],  $A$  the area of the structure [cm<sup>2</sup>]. The Flat-Band Voltage parameter ( $V_{FB}$ ) has been determined by a graphical method [16], which consists in extrapolating the linear part of the following characteristic when the slope crosses the voltage axis:

$$\left[ \left( \frac{C_{OX}}{C} \right)^2 - 1 \right] (\text{Voltage}) \quad (2)$$

A negative charge density of  $9.9 \cdot 10^{+11}/\text{cm}^2$  has been calculated which is consistent with the value given by the glass powder supplier which is  $1 \cdot 10^{+12}/\text{cm}^2$ .

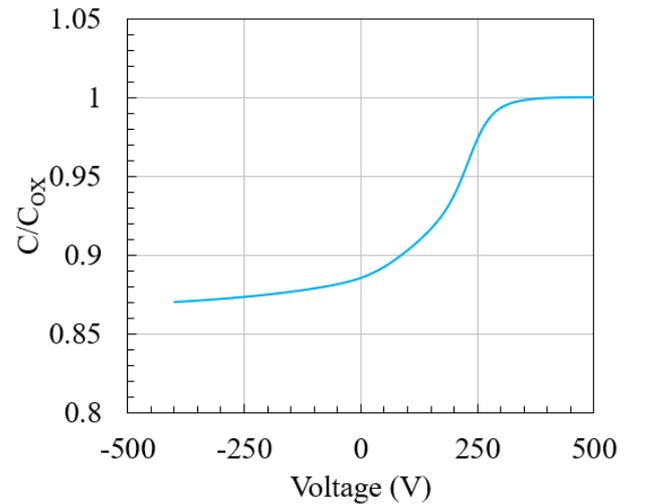


Fig. 6. CV measurement of an MGS Structure between -500 V and 500 V at ambient temperature with a new silicate glass

#### 4.2. Voltage stress effect in MGS structure

Figure 7 exhibits the flat-band voltage of Metal Glass Semiconductor structures over time evolution for different stress voltage after BTS tests. The curves are composed of different sections defined by an increase or a decrease of the flat-band voltage parameter. The first section corresponds to the decrease of the flat-band voltage parameter and can be well observed when the structure is stressed at 100°C. The phenomenon is too fast to be monitored at 125°C and 150°C. Another decrease of the flat-band voltage parameter, identified as the third section, occurred at the end of the test. The second section which corresponds with the increase of the flat-band voltage parameter is observed on the three curves.

The voltage acceleration effect in the range between 300V to 700V does not seem to be significant, however, the absolute variation of flat-band voltage is much important as the electrical field is higher. This behavior confirms the choice to ignore voltage acceleration effects on TRIAC devices.

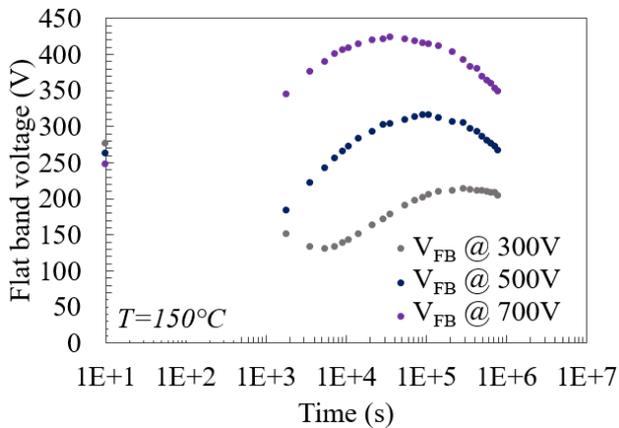


Fig. 7.  $V_{FB}$  parameter evolution over time in MGS structures for three different stress voltages with the new silicate glass. The temperature stress is 150°C

#### 4.3. Temperature stress in MGS structure

Figure 8 shows the flat-band voltage parameter evolution over time of Metal Glass Semiconductor structures for different temperature stresses after BTS tests. As a matter of fact, the curves can also be separated in three sections as observed before however, the temperature acceleration effect appears to be more important compared with voltage acceleration effect.

For each curve of figure 8, an arbitrary degradation criterion was defined (red dash line) as the characteristic time for which the flat-band voltage evolution reaches 250 V when the curves increase. The kinetics of the degradation can here be characterized following an Arrhenius law, with an activation

energy of 0.9eV (fig.10). Hence, the evolution of the flat-band voltage parameter described before might be attributed to the presence of mobile ions [17].

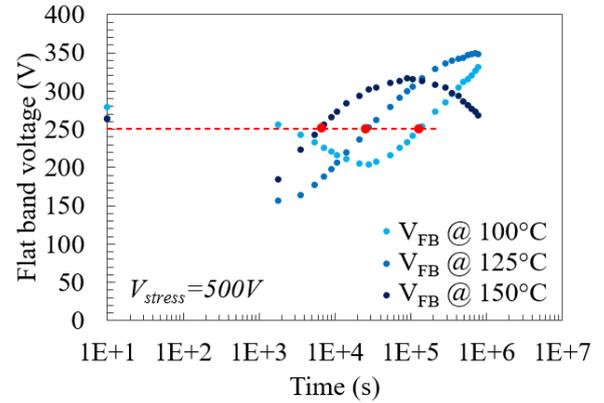


Fig. 8.  $V_{FB}$  parameter evolution over time in MGS structures for three different stress temperatures with the new silicate glass. The voltage stress is 500 V and the red dash line is the degradation criterion

#### 4.4. Temperature stress in TRIAC devices

Figure 9 shows the leakage current drift evolution of TRIAC devices for different temperature levels during HTRB tests. Three slopes were observed on almost all curves. A low slope appears at the beginning of the curves followed by an important slope and once again, a low slope at the end of the curves.

The leakage current drift turns out to be accelerated as the temperature increases. For each curve, a characteristic time, at 30% of leakage current drift, has been extracted (red dash line). The mechanism is activated by the temperature and follows Arrhenius law with an activation energy of 0.9eV (fig.10).

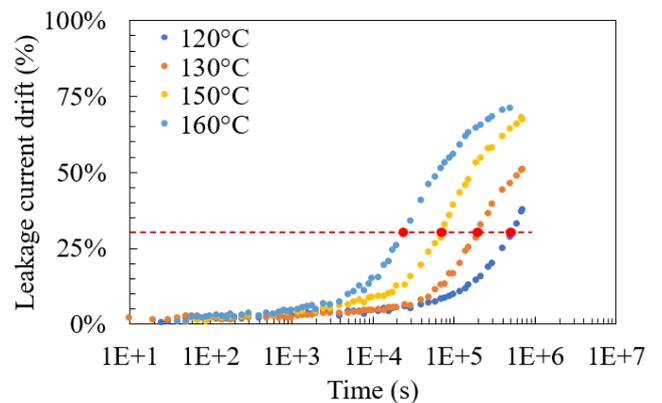


Fig. 9. Leakage current drift of TRIAC devices evolution over time with new glass passivation for different stress temperatures. The voltage stress is 100 V and the red dash line is the degradation criterion

The beginning of the drift after 2 h of stress observed on Metal Glass Semiconductor structures and TRIAC devices seem to be related to the same mechanism. The accumulation of mobile ions near the interface between the new glass and the silicon might be at the origin of the deterioration of the reliability performances as observed elsewhere [17].

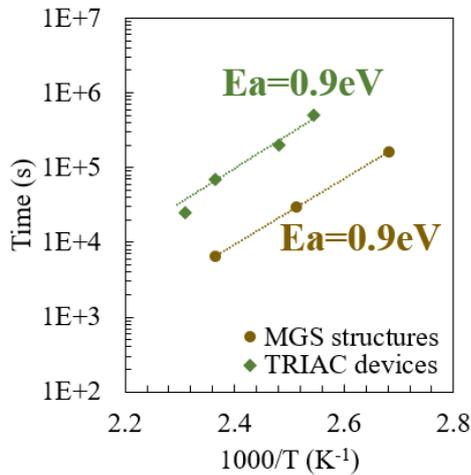


Fig. 10. Arrhenius plot of temperature activated mechanism of MGS structure and TRIAC devices

#### 4.5. Reliability performance improvement with the semi resistive layer

Since the origin of degradation is supposed to be at the glass-silicon interface, a semi-insulating passivation layer was deposited between the new glass passivation and the silicon. Figure 11 shows the leakage current drift evolution over time in TRIAC devices. A DC HTRB test was performed with the same conditions of stress, no leakage current drift has been observed with the presence of the semi-insulating layer. Wang *et al.* [7] reported that the surface of silicon directly passivated with the semi-insulating passivation layer induced charges of opposite polarity near the silicon surface due to its high density of states. Consequently, the induced charges either neutralize the external charges or form a space charge region within the passivated layer. The addition of this semi-insulating passivation layer is of great interest as it seems to trap mobile ions from accumulating near the glass-silicon interface [7], [18]. Therefore, very promising reliability performances are obtained with this semi-insulating passivation layer.

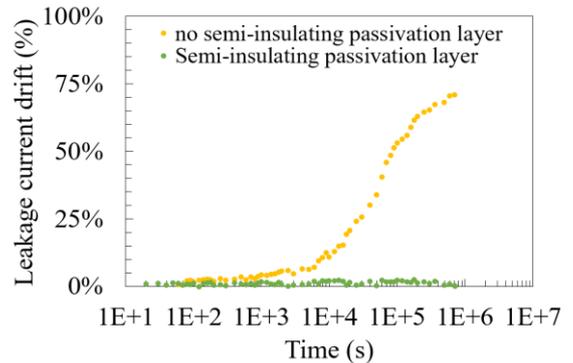


Fig. 11. Leakage current drift evolution over time of TRIAC devices when a semi-insulating passivation layer is deposited between the new silicate glass and the silicon. The voltage stress is 100V and the temperature stress is 160°C

## 5. Conclusion

Dedicated Metal Glass Semiconductor structures and TRIAC devices containing new silicate glass as a passivation layer were studied by means of electrical and temperature stress. Flat-band voltage drift for MGS structures and leakage current drift for TRIAC devices seems to be related to the accumulation of mobile ions near the interface of the glass and the silicon. A semi-insulating passivation layer between the glass and the silicon improves reliability performances as the traps present in semi-insulating passivation layer prevent the mobile ions to accumulate near the glass-silicon interface. This semi-insulating passivation layer is well suitable for high power and high temperature devices and opens up the field of possibilities for exploring new types of glass.

## References

- [1] N.Pal *et al.*, Proceedings of ICETECT, India, Mar 2011
- [2] Y.Shin *et al.*, ICEE Asia, Korea, May 2019
- [3] S.Menard *et al.*, Nanoscale Research Letters, 7:566, 2012
- [4] B.Lu *et al.*, IEEE Trans el dev, Vol.65, No.2, Feb 2018
- [5] S.Jacques *et al.*, AIME, Vol.2, Issue 3, Jul 2014
- [6] Y. Matsumoto *et al.*, ICEEE, Mexico, pp.223-226, 2005
- [7] Y.Wang *et al.*, Microelec. Reliability, 45, pp535-539, 2005
- [8] E.H.Snow *et al.*, J.Appl Phys, vol36, 5, pp.1664-1673, 1965
- [9] G.L. Schnable *et al.*, J. Electrochem.Soc, Vol.122, No.8, Aug 1975
- [10] Y. Misawa, J. Electrochem.Soc, Vol.131, No.8, Aug 1984
- [11] Y. Misawa *et al.*, J. Electrochem.Soc, Vol.128, No.3, Mar 1981
- [12] M. Shimbo *et al.*, IEEE Trans el dev, Vol.35, No.1, Jan 1988
- [13] C.T. Sah *et al.*, IRE Trans el dev, Vol.9, pp. 94-108, Jan. 1962
- [14] L.Lantz *et al.*, Microelec. Reliability, 42, pp1163-1170, 2002
- [15] E.H. Nicollian *et al.*, MOS Physics and Technology, 2003
- [16] K.Piskorski *et al.*, MIPRO, Croatia, May 2010
- [17] M. Shimbo *et al.*, J. Electrochem.Soc, Vol.134, No.1, Jan 1987
- [18] T.Matsushita *et al.*, IEEE Trans el dev, Vol.23, No.8, Aug 1976