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# High Q Zero Level Packaged RF-MEMS Switched Capacitor Arrays

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**Abstract**—This paper presents the design, the realization and the measurement of a thin-film packaged RF-MEMS switched capacitors. Packaging is included in microelectronics fabrication process, with Silicon Nitride thin film. The capacitors are actuated by deflecting thin gold metal membrane towards the package dielectric, increasing the capacitance by a factor 2.47. The device size, including its packaging, is  $80 \times 90 \mu\text{m}^2$ . The highest quality factor of a single capacitor is 1515 at 5 GHz, which comes from the low parasitic capacitance and the thick metallization. To obtain larger capacitance value, an array of  $4 \times 2$  capacitors has been realized and measured.

**Keywords**—Microelectromechanical systems, Package, RF-MEMS, High-Q.

## I. INTRODUCTION

Due to the ever-increasing demand for wireless data access, reconfigurable devices RF components are more and more needed. With the growing number of telecommunication standards, reconfigurable and tunable front ends are needed to limit the complexity of radio front ends. Switched RF-MEMS capacitors are among the serious candidates to realize this function thanks to their low losses, high linearity and very low power consumption compared to semiconductors [1].

Single RF MEMS devices can be combined into pseudo digital arrays of switched capacitors, with combinations resulting in well-defined step variations with high linearity and low loss. Other technologies, like series combination of stacked gate MOS transistors switches with fixed capacitors can be used for the same purpose. These semiconductor technologies offer moderate  $Q_s$ , but they can be made at very low cost, and are very easy to integrate in PC-board RF-circuits.

Indeed, considerations like cost, size, and easiness of integration are critical to the success of RF-MEMS technology. In particular, specific MEMS packaging has been one of the main roadblock against rapid and successful adoption of this technology.

Hermetic wafer-to-wafer bonding with glass-frit intermediate bond layer has successfully been used on commercial switches, but the thickness and profile of the resulting components make them difficult to integrate as surface-mounted elements. Moreover, these packaging techniques are very specific to MEMS and are difficult to insert in low cost CMOS fabrication process flow [2], [3].

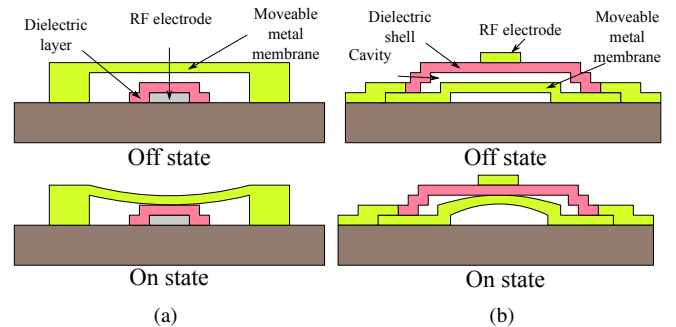


Figure 1. Operating principle of a conventional RF-MEMS capacitive switch (a) and proposed switched capacitor (b).

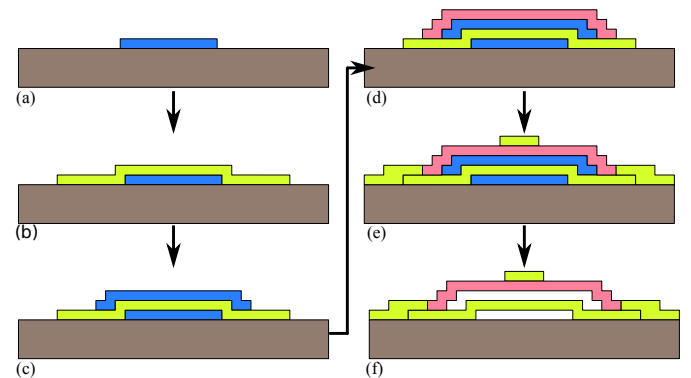


Figure 2. Fabrication steps of the switched capacitor.

Low processing effort and MEMS-unspecific packaging techniques are of high interest for the progress of this technology. There have been several efforts in the past towards the development of low cost, low profile thin film packaging. The idea is to use thin film processing steps for building dielectric shells above micro-electromechanical parts. Most proposed concepts in RF-MEMS stem from early work presented in [4], [5], and have been further developed in [6]–[8], on various ohmic contact and capacitive RF-MEMS structures.

The structures presented in this paper are using miniature RF-MEMS capacitive structures [9]–[11], integrated into silicon nitride dielectric shells. The compactness of the proposed components reduces sensitivity to temperature variations and will permits the integration of compact switched capacitors

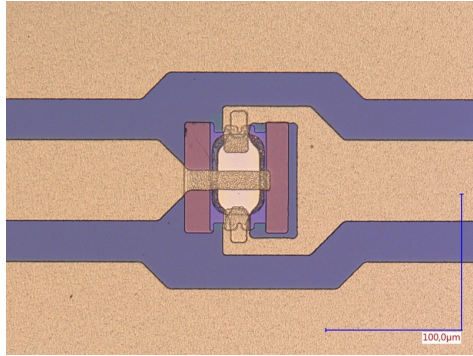
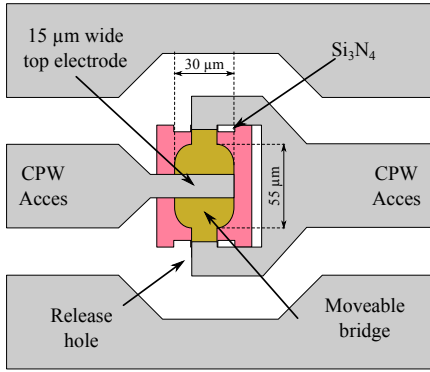


Figure 3. Top view (a) and microphotography (b) of a fabricated switched capacitor.

arrays, which permits to obtain large capacitor values or digitally tunable capacitors (DTC).

## II. FABRICATION

A cross section of the proposed switched capacitor is shown in Fig. 1 along with a sketch of a conventional capacitive switch. In the proposed design, the RF signal electrode is standing above the deflectable metal membrane, and the dielectric layer is also used as a protective shell for the structure.

The processing steps are shown in Fig. 2. Switched capacitors have been fabricated on 400 μm thick silicon substrate, on which a 500 nm thick thermally grown SiO<sub>2</sub> on both sides.

Processing starts with the deposition and patterning of a first 300 nm thick sacrificial layer (Fig. 2a). Next, a 5 nm/400 nm Ti/Au membrane metal, with tensile stress, is evaporated and patterned. Then a second 300 nm thick sacrificial layer is deposited and patterned (Fig. 2b and c). A 500 nm thick Si<sub>3</sub>N<sub>4</sub> layer is then deposited on top of the previous layers and the good conformal properties of the PECVD deposition techniques allowing maintaining good rigidity of the structure (Fig. 2d). Small holes have been etched on the side of the dielectric shells to permit the release of the structure. The last metal layer consists of a low-stress gold layer. Firstly, a 5 nm/200 nm Ti/Au seed layer is deposited by evaporation, then 1 μm of gold is electroplated in order to obtain thicker metallization. This metal layer also allows us to realize the top electrode and the CPW lines used for the switch (Fig. 2e).

Table I. SWITCHED CAPACITOR CHARACTERISTICS.

Beam length $l$	55 μm
Beam width $w$	30 μm
Pull-in voltage $V_p$	25 V (Meas.) / 29 V (Sim.)
Release voltage $V_r$	17 V (Meas.)
Mechanical resonance frequency	1.01 MHz (Sim.)
Switching times @ 1.5V <sub>p</sub>	384 ns (Sim.)
On-state capacitance	52 fF (Meas.)
Off-state capacitance	21 fF (Meas.) / 20 fF (Sim.)

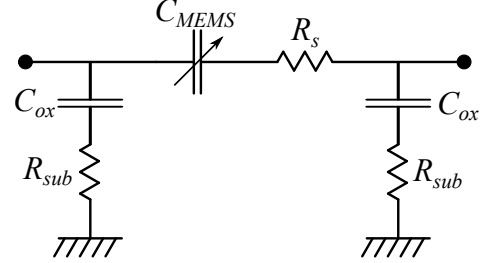


Figure 4. Equivalent scheme of the switched capacitor.

Finally, the sacrificial layers have been etched away, the devices are dried in a critical point drying system. The volume of the fabricated cavities is about 1.5 pL, which is extremely small compared to other packaging techniques for RF-MEMS.

The switch dimensions are given in Fig. 3. The active area is only 75 × 80 μm<sup>2</sup>, including package. The moveable beam is 55 μm long by 30 μm wide. FEM and analytical [1] computed characteristics are summarized in Table I.

The devices have been simulated using ADS, and an equivalent scheme (Fig. 4) has been fitted to measurements. The silicon resistivity adds a significant amount of loss at the access, and this phenomenon has been fitted using conventional CMOS access model.

## III. MEASUREMENTS

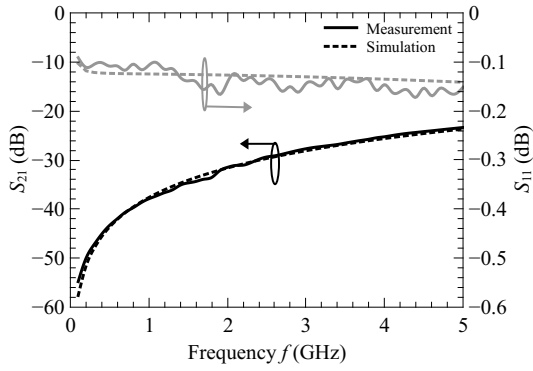
### A. Single capacitor

The measured  $S$ -parameters are shown in Fig. 5 along with equivalent scheme modelling. No de-embedding has been performed on the presented measurements, and the presented results include gold pads to RF probe loss, and access pads substrate losses.

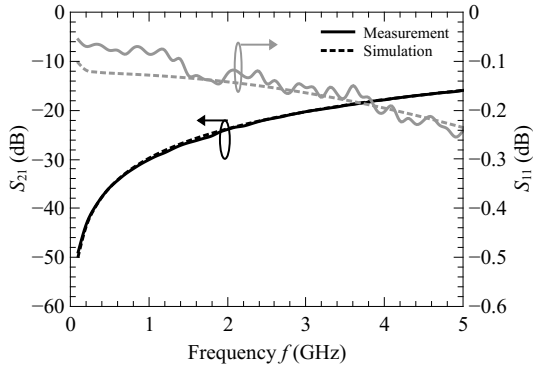
The devices have been biased using 1 kHz bipolar square waveform. When the bias voltage is applied, the extracted capacitance is 52 fF and when the bias voltage is removed, the capacitance value goes back to 21 fF, which is in good agreement with ADS Momentum simulations (Table I, 20 fF). The corresponding contrast is 2.47. The on state capacitance could not be predicted accurately by EM simulation because of the roughness of the dielectric layer. The series resistance  $R_s$  of the capacitor switch is quit hard to extract since the major part of the losses comes from the probe-pads but the value is less than 1 Ω. This permits to computed the quality factor with the following definition:

$$Q = \frac{1}{R_s C_{MEMS} \omega} \quad (1)$$

This gives a quality factor at 5 GHz, of 1515 for the unbiased state and of 612 for the biased state. This high  $Q$



(a)



(b)

Figure 5. Measured (solid line) and equivalent scheme (dashed line) responses of the single capacitor.  $C_{ox} = 0.5$  pF,  $R_{sub} = 7$  k $\Omega$  and  $R_s = 1$   $\Omega$ .  $C_{MEMS}$  is 52 fF in the on-state and 21 fF in the off-state.

comes from the relatively thick metallization (400 nm for the beam and 1.2  $\mu$ m for the top metal). Moreover, the the very low parasitic capacitance (around 6 fF), due to the structure of the MEMS, permits to conserve significant tunability factor with low capacitance value and obtain a high  $Q$ .

The measured pull-in voltage is 25 V, in good agreement with analytical computation [1] (Table I, 29 V), and the release voltage is 17 V.

### B. Capacitor array

A single packaged MEMS capacitor having a small capacitance value, a capacitor array has been design with 8 unit elements assembled in parallel (Fig. 6). Each capacitor has the same characteristics than the single capacitor describes previously. The equivalent modelling scheme is the same for the array since the connexion lines are quite small and do not add parasite inductance in the considered frequency range. The equivalent capacitor of the array is 400 fF in the on-state and 173 fF in the off-state which corresponds to 8 times the capacitance of the single capacitor. The tunability factor of the array is 2.3 which is slightly lower than the capacitor one which may comes to the parasitic capacitances between beam and lines. Thanks to relatively thick top metallization made of gold, the equivalent series resistance stay very low ( $< 1.5$   $\Omega$ ).

## IV. CONCLUSION

A novel switched capacitor has been designed, fabricated and tested. Extremely small packaging has been integrated

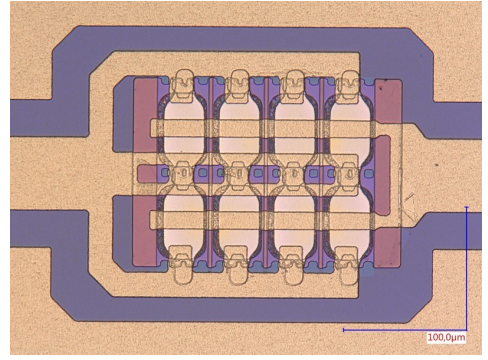
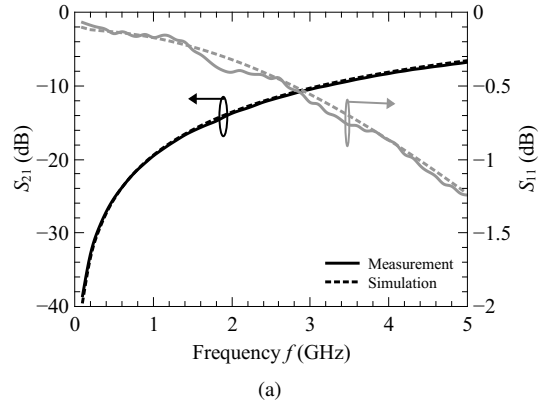
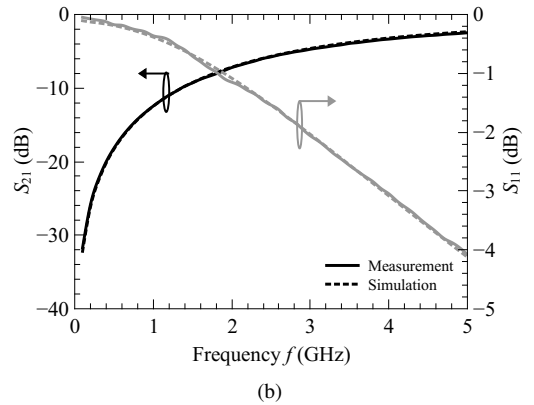


Figure 6. Optical photograph of the capacitor array.



(a)



(b)

Figure 7. Measured (solid line) and equivalent scheme (dashed line) responses of the capacitor array.  $C_{ox} = 0.5$  pF,  $R_{sub} = 7$  k $\Omega$  and  $R_s = 1.5$   $\Omega$ .  $C_{MEMS}$  is 400 fF in the on-state and 173 fF in the off-state.

in the fabrication process, using standard microelectronics processing steps. The capacitor can be switched between 21 and 52 fF, and can be put into arrays of devices in order to obtain compact digital-like variable capacitors. The measured capacitance contrast is 2.47 but it can be easily increased by adding a third electrode to obtain a tri-plate configuration as proposed in [11]. The measured quality factor at 5 GHz of the single capacitor is respectively 1515 and 612 for the unbiased and the biased states, which is one order of magnitude higher than semiconductor technologies. The single capacitor has been successfully integrated into a 4  $\times$  2 shunt capacitor array which permits to obtain a larger values of the capacitance and paves the way to digitally tunable capacitor.

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